

PTO/SB/51 (02-01)

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REISSUE APPLICATION DECLARATION BY THE INVENTOR

Docket Number (Optional)

VN734R1

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is described and claimed

in patent number 5,594,734, granted January 14, 1997, and for which a reissue patent is sought on the invention entitled Asynchronous Processor Access to a Switch Table

Table in a Network With Isochronous Capability
the specification of which

☐ is attached hereto.

☒ was filed on Jan. 14, 1999 as reissue application number 09 / 231,855
and was amended on 01/11/2001

(If applicable)

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, such must be stated with an explanation as to the nature of the broadening:

by reason of claiming only the subject matter of claims 1-18, which is less than the full right to claim in the original application. Accordingly, new claims 19-140 were added. For example, comparing claim 19 to claim 1: claim 1 recites [i]n a computer-controlled system having a microprocessor operating according to a clock and an updatable table operating asynchronously of said clock, said updatable table outputting control data for controlling data transfer in said system, apparatus for updating said updatable table, comprising, while claim 19 recites [i]n a computer controlled system having a processor operating according to a clock and an updatable table operating asynchronously of the clock, the updatable table outputting control data for controlling data transfers in the system, an apparatus, comprising; claim 1 recites register means for receiving update data from said microprocessor during a first time period at a data rate corresponding to said clock and outputting said update data to said updatable table, while claim 19 recites a memory receiving update data from the processor during a first time period at a data rate corresponding to the clock and outputting the update data to the updatable table; and claim 1 recites means, coupled to said register means, for determining the beginning of a second period of time during which said updatable table is not being used and for updating said updatable table during said second period, asynchronously with said clock, using at least some of said update data, while claim 19 recites a control circuit coupled to the memory, wherein the control circuit determines the beginning of a second period of time during which the updatable table is not being used and updates the updatable table during the second period, asynchronously with the clock, using at least some of the update data. Similar errors of claiming less than Applicant was entitled to claim can be seen from the subject matter of new claims 20-140, which include subject matter that Applicant was entitled to claim but did not in the original application.

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(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)

VN734RI

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant. As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

Name(s)

Registration Number

Alan R. Loudermilk

32,788

Correspondence Address: Direct all communications about the application to:



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Address	Suite B				
City	Cupertino	State	CA	Zip	95014
Country	USA				
Telephone	408-342-1866	Fax	408-342-1868		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of sole or first inventor (given name, family name)

DEBRA J. WORSLEY

Inventor's signature

Date

Residence

Citizenship

Mailing Address

Full name of second joint inventor (given name, family name)

MICHAEL T. WERSTLEIN

Inventor's signature

Date

Residence

Citizenship

Mailing Address

3242 SW 34th St., REDMOND, OR 97756

Full name of third joint inventor (given name, family name)

RICHARD W. THAIK

Inventor's signature

Date

Residence

Citizenship

Mailing Address

☐ Additional joint inventors are named on separately numbered sheets attached hereto.

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Registration Number

Alan R. Loudermilk

32,788

Correspondence Address: Direct all communications about the application to:



Customer Number

Type Customer Number here

Place Customer Number Bar
Code Label here

<input checked="" type="checkbox"/> Firm or Individual Name	Loudermilk & Associates				
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Address	Suite B				
City	Cupertino	State	CA	Zip	95014
Country	USA				
Telephone	408-342-1866	Fax	408-342-1868		

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Full name of sole or first inventor (given name, family name)

DEBRA J. WORSLEY

Inventor's signature

Date

Residence 1723 W. Hedding St.

Citizenship

Mailing Address San Jose, CA 95126

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MICHAEL T. WERSTLEIN

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Date

Residence Same as below.

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